RollNo.

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, Nov- Dec 2024

BTech IT
III Semester
IT23301 - DIGITAL LOGIC DESIGN
(Regulation 2023)

Time:3hrs Max.Marks: 100

CO1	Simplify complex Boolean functions.
CO2	Implement digital circuits using combinational logic ICs.
CO3	Design digital circuits with various combinational logic and write HDL for digital system.
CO4	Understand the characteristics of various sequential circuits with combinational circuits
CO5	Design and implement various programmable logic devices.

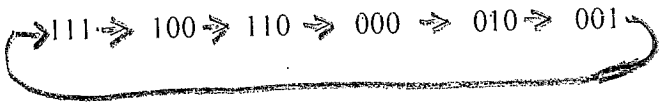
BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

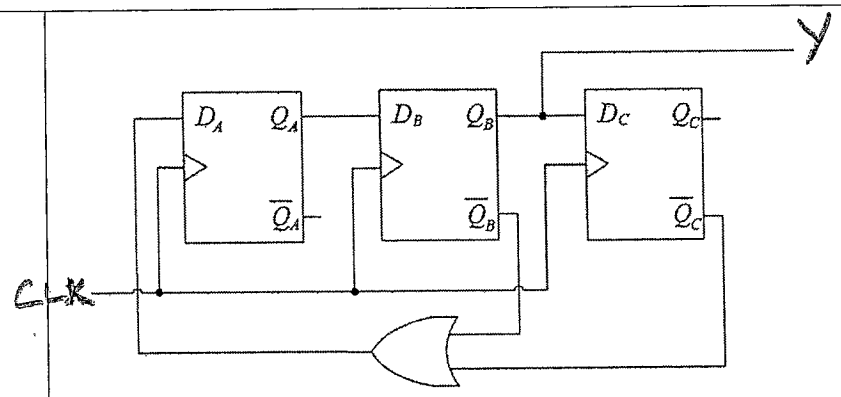
PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	Simplify the given Boolean function $y(x+y')$	2	CO1	L2
2	Draw logic diagram for $F(x,y,z)=xy+y'z$	2	CO1	L3
3	Simplify using k-map AB/CD x x 1 x 0 0 1 x 0 0 x x x 1 1 1	2	CO2	L3
4	Simulate (HDL) using gate level modeling of $F(x,y,z)=(x+y)(x'+z)$	2	CO2	L2
5	Write the truth table for 4 x 2 low priority encoder	2	CO3	L2
6	Find $(58)_{10}$ equivalent code in BCD and 84-2-1 codes	2	CO3	L3
7	A 3 bit right shift register operation as $S_{in} \rightarrow X \rightarrow Y \rightarrow Z$. If present state of register is 100 and S_{in} is 1, find the number of clock cycles required to reach the state XYZ is 111	2	CO4	L3
8	Compare moore and mealy models with block diagram	2	CO4	L2
9	Draw logic circuit of basic binary memory cell	2	CO5	L1
10	Find even parity bit appended for the code 1000101 Justify your answer and explain how is it useful for error detection	2	CO5	L2

PART- B(5x 13=65Marks)
(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks	CO	BL
11 (a) (i)	Perform binary subtraction using 1's complement and 2's complement for (27 -18)	4	CO1	L3

(ii)	Find minterm and maxterm for the given the function $F(A,B,C)= C'+AB'$ Give truth table and draw logic circuit	9		
	OR			
11 (b) (i)	Draw logic circuit using NAND gates only for $F= (x+y)(y'+z)$	4	CO1	L3
(ii)	Given the function $F(w,x,y,z)= \sum(0,1,2,3,8,9,10,11,13)$ $Dontcares=\sum(4,5,7,14,15)$ Simplify the function , Draw logic circuit and provide truth table	9		
12 (a) (i)	Design a 3 x 2 multiplier circuit and draw block/logic diagram	4	CO2	L3
(ii)	Design a fast adder for adding two 4-bit binary numbers, focusing on speeding up carry propagation. Justify speeding up.	9		
	OR			
12 (b) (i)	Design a full subtractor. Draw circuit and provide truth table	4	CO2	L2
(ii)	Design a circuit to determine the majority vote among three voters A,B,C (output is one if two or more inputs are one).	9		L3
13.a (i)	Design 16 x 1 multiplexer using 4x 1 mux	4	CO3	L3
(ii)	Design a combinational circuit that generates 9s complement of a BCD digit	9		
	OR			
13 (b) (i)	Design a two bit comparator to check A=B ? and A< B?	4	CO3	L3
(ii)	Design a BCD to 8 4 -2 -1 code converter and draw logic circuit	9	CO3	L3
14 (a) (i)	Design a 3 bit shift left and parallel input register	4	CO4	L3
(ii)	Design a synchronous counter using T flip-flop with the following sequence 	9		
	OR			
14 (b) (i)	Design a mod 5 up counter using T Flip flops	4	CO4	L3
(ii)	Analyse the given sequential circuit . write state table, and state diagram	9		L4

				
15 (a) (i)	(i) Draw internal logic of a 16 x 8 ROM diagram. How many address lines needed for 64k x 8 memory. How this addressing is achieved in real memory.	4	CO5	L2
(ii)	(ii) Tabulate the PLA programming table and implement the three Boolean functions such that you minimize the number of product terms to deploy the circuit. A(X,Y,Z) = Σ (1,2,3,4,5) B(X,Y,Z) = Σ (0,1,5,7) C(X,Y,Z) = π (2,3,7)	9	CO5	L3
	OR			
15 (b) (i)	Discuss about sequential programmable devices.	4	CO5	L2
(ii)	Tabulate the PAL programming table and implement the three Boolean functions such that you minimize the number of product terms to deploy the circuit. A(X,Y,Z) = Σ (1,3,4,5,7) B(X,Y,Z) = Σ (0,1,2,3,6) C(X,Y,Z) = π (2,3,5,6).	9	CO5	L3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16.	An Arithemetic unit should perform following jobs 1. Complementing n bit number 2. Providing 2's complement 3. Incrementing by one bit (a=a+1) 4. Decrementing by one bit(a=a-1) 5. Multiplying with 2 (a=a x 2) 6. Producing interleaved numbers (1,3,5,7..) Design the system Draw block diagram Draw logic diagram for each block Write HDL code for virtually simulating this system	15	CO1 CO2 C03 CO4 CO5	L6